REMARKS

Claims 4-15 are pending in this application, of which claims 4 and 5 are independent. Acknowledgement is made with appreciation that claims 5-13 and 15 are allowed. This patent application is deemed to be in allowable condition, in light of the following remarks.

The Examiner rejects claims 4 and 14 under 35 USC §103(a) as being unpatentable over the "admitted prior art in the instant application" ("AAPA") in view of Kobayashi, each of which were cited in the previous Office Action. It is noted that the Examiner had indicated that claim 4 would be allowable pending rewriting it in independent form. Following the rewrite, claim 4 has been newly rejected, in this instance. The rejection is respectfully traversed.

The Examiner refers to Fig. 8 of the pending application as AAPA. Fig. 8 illustrates a conventional digital synchronous circuit. As regards claim 4, Fig. 8 does not disclose "a control circuit for generating a control signal after a prescribed period of time according to a change in said input data signal," and the claimed delay circuit connected to receive an output of the pulse signal generating circuit, as claim 4 recites. However, the Examiner relies on Kobayashi for teaching these missing features.

Kobayashi alleges to overcome the problem of latching an unstable data signal in the following manner. Fig. 2B of Kobayashi shows generally a "data transfer device," which includes a latch control circuit 7, which generates a data latch signal DL in accordance with an externally-supplied latch control signal LC and data D supplied from data transfer circuit 6. Also shown is data latch circuit 8, which latches data D transferred from data transfer circuit 6 in response to a rising point of change of data latch signal DL. Generation of the data latch signal DL can be seen in the time diagram of Fig. 5. While the data latch signal DL is generated in accordance with the input data signal D and the transfer signal TR, referring to this timing

diagram, the control signal DL1 and DL3 are output after a period of time according to a change of the input data signal D. It is alleged that this avails latching of unstable data.

On pages 2-4 of the Office Action, the Examiner reiterates grounds of rejection in accordance with cancelled claim 1, but acknowledges that Kobayashi does not disclose a control circuit included in the pulse generating circuit *followed* by a delay circuit, as claim 4 requires. However, the Examiner alleges that as Kobayashi discloses a delay circuit followed by a pulse generating circuit, it would have been obvious to reverse the order of the pulse generating circuit and delay circuit "because such modification won't have any impact on the operation of the latched circuit." The cited motivation is flawed, rendering the claim rejection improper.

It is firmly established that even if prior art could have been modified so as to result in the combination defined by the claims, for the modification to be obvious, there must be a suggestion of the desirability of the modification. *See In re Deminski*, 796 F.2d 436 (Fed. Cir. 1986). Simply because the modification allegedly "won't have any impact on the operation of the latched control circuit" in no way suggests a desirability of modification. Moreover, requisite motivation must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *See In re Newell*, 891 F.2d 899 (Fed. Cir 1986). However, the motivation asserted by the Examiner does not establish why one would have realistically been impelled to reverse the order of the pulse generating circuit and delay circuit, nor has the motivation established a reasonable expectation of achieving any specific benefit. In light of the foregoing, simply stating that such modification "won't have any impact on the operation of the latch control circuit" has no relevance.

The Examiner has failed to establish any motivation to combine AAPA in view of Kobayashi for arriving at the claimed invention, and as a result, has not met a burden of proof. Claim 14 is patentable at least based on dependency to independent claim 4. Withdrawal of the rejection is respectfully solicited.

In section 5 of the Office Action, the Examiner objects to the drawings under 37 CFR §1.83(a). The Examiner alleges that "a pulse generating circuit for generating a pulse signal" and "a delay circuit for receiving said pulse signal to cause delay" in claim 4 is not shown in the drawings, and asserts that these claimed features must be cancelled from the claims. To the contrary, the written description of the specification clearly explains the claimed configuration. Description can be found on pages 13-14, lines 27-3, respectively, of the specification. Furthermore, Figs. 4, 6 and 7 illustrate a pulse generating circuit 43 for generating a pulse signal and a latch control circuit 40a-c, respectively (*i.e.,* comparator 4011), for providing delay. As the claimed features are clearly illustrated by the drawings, drawing corrections or amendments are not required. Withdrawal of the drawing objection is respectfully solicited.

If the Examiner has any comments regarding the application in general or this response, he is encouraged to contact the undersigned in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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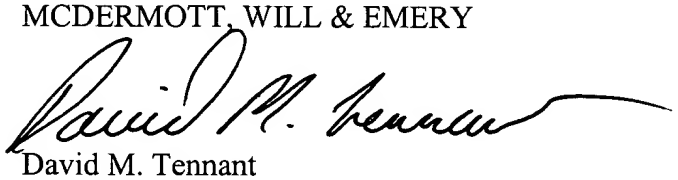

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Date: April 7, 2004